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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,859	04/14/2004	Hee-Cheol Choi	SAM-0522	6192

7590 06/07/2007

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EXAMINER	
EGAN, SCOTT T	
ART UNIT	**PAPER NUMBER**
2622	

MAIL DATE	DELIVERY MODE
06/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,859	CHOI, HEE-CHEOL	
	Examiner	Art Unit	
	Scott Egan	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 34, 35 and 38 are objected to because of the following informalities: the listed claims are listed with dependence on claim 26, however claim 26 makes no reference to the PGA, therefore the claims will be interpreted as dependent upon claim 32. Appropriate correction is required.

Drawings

2. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: Page 9 line 22 reads "an integer between from 1 to 64" and it is recommended that it be changed to "an integer from 1 to 64".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-11, 13, 15, 16, 18-22, 24, 26, 27, 29-36, 38, 40, 41, 43-47 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al. (US 2002/0176009).

Consider **claim 1**, Johnson et al. explicitly teach:

An image processing system (analog image processing system 113, fig 3), comprising:

an input for receiving an input signal (see fig 3 and 5, Vin); and

a correlated double sampler (CDS) for receiving the input signal (CDS/VGA 114), sampling the input signal and providing an output signal (outputs signal to ADC 116 as seen in fig 3), the CDS comprising an amplifier for amplifying the input signal (amplifier 134, fig 5).

Consider **claim 2**, Johnson et al. explicitly teach:

The image processing system of claim 1, wherein gain in the CDS is settable to one of a plurality of levels (paragraph [0067], lines 22-26).

Consider **claim 4**, Johnson et al. explicitly teach:

The image processing system of claim 1, wherein gain in the CDS is settable to a level between 1.0 and 2.0 (paragraph [0067], lines 22-26, which corresponds to a range of 0 to 10, which could be adjusted to cover the specified range).

Consider **claim 5**, Johnson et al. explicitly teach:

The image processing system of claim 1, wherein gain in the CDS is settable by a digital input signal (paragraph [0067], lines 20-22).

Consider **claim 6**, Johnson et al. explicitly teach:

The image processing system of claim 5, wherein the digital input signal contains a plurality of bits (paragraph [0067], lines 20-22).

Consider **claim 7**, Johnson et al. explicitly teach:

The image processing system of claim 1, further comprising a programmable gain amplifier (PGA) for receiving the output signal from the CDS (CDS/VGA 114) and amplifying the received signal (fig 3 shows the VGA as the second section of the CDS/VGA 114, which includes amplifier 144).

Consider **claim 8**, Johnson et al. explicitly teach:

The image processing system of claim 7, wherein gain in the PGA is settable to one of a plurality of levels (paragraph [0067], lines 22-26).

Consider **claim 9**, Johnson et al. explicitly teach:

The image processing system of claim 7, wherein gain in the PGA is settable to a level between 1.0 and 2.0 (paragraph [0067], lines 22-26, which corresponds to a range of 0 to 10, which could be adjusted to cover the specified range).

Consider **claim 10**, Johnson et al. explicitly teach:

The image processing system of claim 7, wherein gain of the PGA is settable by a digital input signal (paragraph [0067], lines 20-22).

Consider **claim 11**, Johnson et al. explicitly teach:

The image processing system of claim 10, wherein the digital input signal contains a plurality of bits (paragraph [0067], lines 20-22).

Consider **claim 13**, Johnson et al. explicitly teach:

The image processing system of claim 7, wherein an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA (paragraph [0068], lines 18-21).

Consider **claim 15**, Johnson et al. explicitly teaches:

An image processing system (analog image processing system 113, fig 3), comprising:

a correlated double sampler (CDS) for receiving an input signal (CDS/VGA 114), sampling the input signal and providing an output signal (outputs signal to ADC 116 as seen in fig 3), the CDS comprising an amplifier for amplifying the input signal (amplifier 134, fig 5); and

a programmable gain amplifier (PGA) (CDS/VGA 114) for receiving the output signal from the CDS and amplifying the received signal (fig 3 shows the VGA as the second section of the CDS/VGA 114, which includes amplifier 144).

Consider **claim 16**, Johnson et al. explicitly teach:

The image processing system of claim 15, wherein gain in the CDS is settable to one of a plurality of levels (paragraph [0067], lines 22-26).

Consider **claim 18**, Johnson et al. explicitly teach:

The image processing system of claim 15, wherein gain in the CDS is settable to a level between 1.0 and 2.0 (paragraph [0067], lines 22-26, which corresponds to a range of 0 to 10, which could be adjusted to cover the specified range).

Consider **claim 19**, Johnson et al. explicitly teach:

The image processing system of claim 15, wherein gain in the PGA is settable to one of a plurality of levels (paragraph [0067], lines 22-26).

Consider **claim 20**, Johnson et al. explicitly teach:

The image processing system of claim 15, wherein gain in the PGA is settable to a level between 1.0 and 2.0 (paragraph [0067], lines 22-26, which corresponds to a range of 0 to 10, which could be adjusted to cover the specified range).

Consider **claim 21**, Johnson et al. explicitly teach:

The image processing system of claim 15, wherein a gain in the CDS and a gain in the PGA are settable by a digital input signal (paragraph [0067], lines 20-22).

Consider **claim 22**, Johnson et al. explicitly teach:

The image processing system of claim 21, wherein the digital input signal contains a plurality of bits (paragraph [0067], lines 20-22).

Consider **claim 24**, Johnson et al. explicitly teach:

The image processing system of claim 15, wherein an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA (paragraph [0068], lines 18-21).

Consider **claims 26, 27, 29-36, 38, 40, 41, 43-47 and 49**, they are corresponding methods of **claims 1, 2, 4-11, 13, 15, 16, 18-22, and 24**, which are identical in scope and therefore are rejected for the same reasons as the apparatus claims above.

5. **Claims 1, 3, 15, 17, 26, 28, 40, and 42** rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (US 6,388,500).

Consider **claim 1**, Lee et al. explicitly teach:

An image processing system (gain controller using switched capacitors), comprising:

an input for receiving an input signal (REF and DATA in figure 7); and

a correlated double sampler (CDS) for receiving the input signal (correlated double sampler 82), sampling the input signal and providing an output signal, the CDS comprising an amplifier for amplifying the input signal (units 90 and 92).

Consider **claim 3**, Lee et al. explicitly teach:

The image processing system of claim 1, wherein gain in the CDS is settable to one of four levels (column 5, lines 39-45).

Consider **claim 15**, Lee et al. explicitly teach:

An image processing system (analog image processing system 113, fig 3), comprising:

a correlated double sampler (CDS) for receiving an input signal (correlated double sampler 82), sampling the input signal and providing an output signal, the CDS comprising an amplifier for amplifying the input signal (units 90 and 92); and

a programmable gain amplifier (PGA) (gain controller 84) for receiving the output signal from the CDS and amplifying the received signal (column 5, lines 39-45).

Consider **claim 17**, Lee et al. explicitly teach:

The image processing system of claim 15, wherein gain in the CDS is settable to one of four levels (column 5, lines 39-45).

Consider **claims 26, 28, 40 and 42**, they are corresponding methods of **claims 1, 3, 15, and 17**, which are identical in scope and therefore are rejected for the same reasons as the apparatus claims above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 12, 14, 23, 25, 37, 39, 48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al.

Consider **claim 12**, in one embodiment Johnson et al. explicitly teach:

The image processing System of claim 11, wherein the gain levels are controlled by an 8 bit word.

However, Johnson et al. does not specifically teach in the particular embodiment that the first portion of bits are used to control the CDS and the second portion of bits are used to control the VGA.

In the same field of endeavor, another embodiment of Johnson et al. teaches a splitter 197 that splits an overall gain signal into more than one in fig 11. It is interpreted that this split corresponds to the first portion of the 8 bit word being split to the CDS and the second portion of the 8 bit word being split to the VGA.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the splitter found in fig 11 into the AIPS to split the signal from the AGC controller 119 to the CDSVGA in order to save space and money in eliminating the necessity of multiple controllers if the signal is not split.

Consider **claim 23**, in one embodiment Johnson et al. explicitly teach:

The image processing System of claim 22, wherein the gain levels are controlled by an 8 bit word.

However, Johnson et al. does not specifically teach in the particular embodiment that the first portion of bits are used to control the CDS and the second portion of bits are used to control the VGA.

In the same field of endeavor, another embodiment of Johnson et al. teaches a splitter 197 that splits an overall gain signal into more than one in fig 11. It is interpreted

that this split corresponds to the first portion of the 8 bit word being split to the CDS and the second portion of the 8 bit word being split to the VGA.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the splitter found in fig 11 into the AIPS to split the signal from the AGC controller 119 to the CDSVGA in order to save space and money in eliminating the necessity of multiple controllers if the signal is not split.

Consider **claims 37 and 48**, they are corresponding methods of **claims 12 and 23**, which are identical in scope and therefore are rejected for the same reasons as the apparatus claims above.

Consider claim 14, Johnson et al. explicitly teach the image processing system of claim 13.

However, Johnson et al. do not explicitly teach that the overall gain is pseudo-logarithmic.

Official notice is taken that both the concept and advantages of providing for pseudo-logarithmic gain are well known and expected in the art. It would have been obvious to include pseudo-logarithmic gain into the analog image processing system found in Johnson et al. in order to accommodate for a wide range of input signals.

Consider claim 25, Johnson et al. explicitly teach the image processing system of claim 24.

However, Johnson et al. do not explicitly teach that the overall gain is pseudo-logarithmic.

Official notice is taken that both the concept and advantages of providing for pseudo-logarithmic gain are well known and expected in the art. It would have been obvious to include pseudo-logarithmic gain into the analog image processing system found in Johnson et al. in order to accommodate for a wide range of input signals.

Consider **claims 39 and 50**, they are corresponding methods of **claims 14 and 25**, which are identical in scope and therefore are rejected for the same reasons as the apparatus claims above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fowler (US 6,757,018) teaches and amplifier with gain controlled by the 5 digital bits. Holberg et al. (US 6,720,999) teaches a CCD analog processor system with a CDS and VGA including four different levels of gain settings.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Egan whose telephone number is (571) 270-1452. The examiner can normally be reached on Monday-Friday 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SE

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER